A METHOD FOR MAKING A TUNGSTEN-PLUG IN AN INTEGRATED CIRCUIT DEVICE WITHOUT VOLCANO PHENOMENA

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The invention relates to a method of making tungsten plugs in integrated circuit devices by a chemical vapor deposition process, and more particularly, to an improvement in the method which eliminates the volcano phenomena. The method of the present invention dramatically increases the efficiency of the method by producing fewer defective devices exhibiting the undesirable volcano phenomena.

2. DESCRIPTION OF THE PRIOR ART

It is widely known that Ti, W, TiN or Al alloys are used for metal interconnection in USLI technology. For example, the double level metal interconnection process used commercially today employs a Ti/TIN/W tri-layer structure to form the first level metal interconnection, in which the Ti is the bottom layer that makes electrical contact with the source and drain electrodes of the Field Effect Transistor devices.

Conventional methods of making the first level metal interconnection in the double level metal interconnection process include the following steps:

(1) Depositing a SiO_2 insulation layer on top of the contact hole and devices by chemical vapor deposition (CVD), then depositing a layer of BPSG (Boronphospliosilicate Glass) onto the SiO2 layer for surface planarization by employing CVD again;

(2) Forming contact holes as shown in Figures 1 and 2;

(3) Making ion implantation through the contact holes and forming the devices;

(4) Sputter depositing a barrier metal layer made up of Ti and TiN, in which the Ti metal is underneath the TiN; the barrier layer crosses the contact holes mentioned above;

(5) Depositing W metal to form the W-plug in the contact hole by plasma anisotropic etchback technique.

Using these methods, the Ti layer is about 300 angstroms thick and the TiN is about 1500 angstroms thick. The following reactions occur to form W metal by CVD:

$$WF_6(g) + SiH4(g) \rightarrow W(s) + SiF_4(g) + H_2(g)$$

$$WF_6(g) + H_2(g) \rightarrow W(s) + HF(g)$$

WF_6 is reacted with SiH4 in the first step of the process. Thereafter hydrogen gas ($H_2(g)$) is reacted with WF_6 which produces tungsten (W).

However, the Ti/TiN layer made in step (4) has a very poor step coverage capability. Therefore the Ti/TiN layer can be very thin near the top and bottom of the sidewalls of the contact holes, as shown in Figure 3. As a consequence of this phenomenon, the WF_6 gas used for W metal deposition will penetrate the TiN layer and react with the Ti metal underneath to produce the evaporative TiF_4, which will result in an explosive phenomena near the contact hole. This is called the volcano phenomena. The reaction of Ti with WF_6 is as follows:

$$Ti(s) + WF_6(g) \rightarrow W(s) + TiF_4(g)$$

This volcano phenomena can easily cause peeling of the Ti, TiN or W layers which makes the devices defective and thereby reduces the yield of acceptable

devices produced by the process.

In addition, the deposited tungsten layer will not adhere to the surface of SiO_2 or BPSG. The TiN layer is deposited before the tungsten layer is formed as a barrier layer to avoid peeling. Since the TiN layer is deposited by sputtering, the volcano phenomenon is even more likely to happen near the edge of the silicon wafer. Because the wafer was held down by a quartz clamp ring inside the reaction chamber, some BPSG will be left near the edge of the wafer. This makes the tungsten nucleation layer insufficient near the edge and thus reduces the reaction speed for the WF_6 gas to produce the tungsten (W) metal. The overabundant WF_6 gas facilitates peeling of the tungsten (W) layer resulting in the production of defective devices which reduces the overall yield of acceptable devices manufactured by the process.

United States Patent 5,489,552 the entire disclosure of which is herein incorporated by reference, relates to a multiple layer tungsten deposition process and discusses the volcano phoneme. United States Patent 5,436,200, the entire disclosure of which is herein incorporated by reference, describes a blanket tungsten deposition process utilizing a ceramic ring.

SUMMARY OF THE INVENTION

In view of the foregoing, the primary object of the present invention is to provide a high yield, low cost and highly efficient manufacturing process for making IC metal interconnections and avoiding the volcano phenomena.

This invention uses two CVD (chemical vapor deposition) chambers with clamp rings of different sizes to control the deposition area and thickness. This approach ensures that the bulk deposition of tungsten (W) is on the nucleation layer. Thus, the penetrating of excessive WF_6 gas into TiN barrier layer is avoided. This prevents the volcano phenomena from happening.

The process of the present invention comprises the following steps:

(1) Depositing a SiO_2 insulation layer (25) on top of a substrate (20) by CVD; and then depositing a layer of BPSG (30) onto the SiO_2 layer (20) for surface planarization by again employing CVD;

(2) Partially etching the SiO_2 insulation layer (25) and the BPSG layer (30) to form contact holes on the substrate (20);

(3) Making ion implantation through the contact hole and forming the devices;

(4) Sputter depositing a barrier metal layer made up of Ti followed by rapid thermal nitridation to form a TiN layer in which the Ti metal is underneath the TiN layer which is bilayer (40);

(5) Depositing tungsten (W) metal in two CVD chambers with different quartz clamp rings to control the area and thickness of the tungsten nucleation layer (50) and bulk deposition area of the tungsten (W) layer (60) in order to ensure the bulk deposition is onto the nucleation layer;

(6) Forming the tungsten-plug in the contact hole by plasma anisotropic etch back technique;

(7) Sputtering on a Al/Si/Cu layer and pattern metal lines by conventional technology.

The rapid thermal nitridation of step (4) may take place at, for example, 760°C for 30 seconds.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings further describe the prior art and the invention.

FIG. 1-3 show the cross-sectional representation of the conventional process for making the first level metal interconnection.

FIG. I shows the cross-sectional representation of the silicon wafer after SiO_2 deposition. The SiO_2 is used as an insulation layer.

FIG. 2 shows the cross-sectional representation after etching unwanted SiO_2 layer to make contact holes. The metal layer will form electrical contact to the devices.

FIG. 3 shows the cross-sectional representation of Ti and TiN deposition by sputtering. These metal layers contact the devices on the silicon wafer through the contact holes in the SiO_2 layer.

FIG. 4 shows the cross-sectional representation of the process of the invention for making the first level metal interconnection.

FIGS. 5A, 5B, and 5C show the top view and cross-sectional view of the three quartz (1, 2, 3) clamp rings of different size used in the CVD process in this invention.

FIG. 6 shows the system of operation procedure with the CVD chamber A and chamber B used in this invention for the deposition of tungsten (W) metal.

DETAILED DESCRIPTION OF THE INVENTION

In the conventional method for making IC, a field contact hole is formed to insulate the active area from the silicon substrate, then the FET is made which contains the gate dielectric, the gate electrode, spacer and source/drain region. Thereafter the metal interconnection process is widely used today and has been described in the field of this invention mentioned above.

This invention improves the process for making the first level metallization in the double level metal interconnection process, to prevent the volcano phenomena and peeling of the metal layer. Fig. 4, depicts the cross-sectional view of the device made by the process of the present invention. The process comprises the following steps:

(1) Depositing a SiO_2 insulation layer (25) on top of a substrate (20) by CVD; and then depositing a layer of BPSG (30) onto the SiO_2 layer (20) for surface planarization by again employing CVD;

(2) Partially etching the SiO_2 insulation layer (25) and the BPSG layer (30) to form contact holes on the substrate (20);

(3) Making ion implantation through the contact hole and forming the devices;

(4) Sputter depositing a barrier metal layer made up of Ti followed by rapid thermal nitridation to form a TiN layer in which the Ti metal is underneath the TiN layer which is bilayer (40);

(5) Depositing tungsten (W) metal in two CVD chambers with different quartz clamp rings to control the area and thickness of the tungsten nucleation layer (50) and bulk deposition area of the tungsten (W) layer (60) in order to ensure the bulk deposition is onto the nucleation layer;

(6) Forming the tungsten-plug in the contact hole by plasma anisotropic etch back technique;

(7) Sputtering on a Al/Si/Cu layer and pattern metal lines by conventional technology.

The rapid thermal nitridation of step (4) may take place at, for example, 760°C for 30 seconds.

Referring now more particularly to Figure 5A for further explaining the critical step (5) in this process. There is shown a wafer 10 in step (4) and it is held down by a quartz clamp ring 1 of 2mm width. This wafer now has BPSG 30 as its top layer. A Ti/TiN bilayer 40 is then sputtered onto the wafer 10, with the result that near the edge of the wafer 10 is a 2mm wide band of the BPSG layer not covered with Ti/TiN 40, but only the BPSG 30 film from the previous step. Thereafter referring now to Figure 5B, tungsten metal is deposited by the following two steps: First, a tungsten nucleation layer 50 is formed on the wafer 10 using CVD in chamber A 90 (referring Fig. 6) by reducing the WF_6 by SiH_4:

$$WF_6(g) + SiH_4(g) \rightarrow 4W(s)+SiF4(g)+H_2(g).$$

The reaction pressure is about between 4.5 to 30 torr and reaction temperature is between 445 to 475° C by Ar with 1000 to 3000 Sccm , N_2 with 300 to 500 Sccm , H_2 with 1000 to 1500 Sccm, SiH_4 with 5 to I0 Sccm and WF_6 with 10 to 20 Sccm.

This nucleation layer 50 is about between 500 to 800 angstroms thick. In this process, the silicon wafer 10 is held down by a quartz clamp ring 2 of 3mm width, thus the ring 2 covers the 2mm wide BPSG 30 layer and an additional 1 mm band of the Ti/TiN bilayer 40. No tungsten metal is deposited onto the BPSG 30 surface and no peeling will occur. Moreover, separating the formation of the nucleation layer 50 and the bulk deposition of tungsten into two CVD chambers enables better control of the nucleation layer thickness, and thus better protection for the Ti/TiN structure underneath.

After this step, referring now to Fig. 5C, the wafer 10 is transferred into CVD chamber B 95 (referring Fig. 6) from chamber A 90 (referring to Fig. 6) and held by a quartz clamp ring 3 which is about 5mm wide, then tungsten metal 60 is bulk deposited onto the tungsten nucleation layer 50 on the wafer 10 with between 7500 to 8000° by reducing WF_6 with H_2 employing CVD and the following reaction:

$$WF_6(g)+H_2(g) \rightarrow W(s)+HF(g)$$

The reaction pressure is about between 70 to 90 torr and reaction temperature is between 445 to 475° C by Ar with 2000 to 4000 Sccm , N_2 with 300 to 500 Sccm , H_2 with 500 to 1500 Sccm and WF_6 with 10 to 20 Sccm.

The tungsten-plug in the contact hole is formed by plasma anisotropic etchback technique.

This is followed by sputtering an Ai/Si/Cu layer and pattern metal lines by etching out unwanted Ti, TiN and Al/Si/Cu employing conventional etching and

lithography technology.

The tungsten nucleation layer 50 made in chamber A 90 (referring Fig. 6) can be used as a passivation layer to prevent the WF_6 penetrating the TiN layer and reacting with Ti to form TiF_4 during the bulk deposition of tungsten in chamber B 95 (referring to Fig. 6). By depositing tungsten using two different quartz claim rings and two chambers facilitates the elimination of the volcano phenomena as mentioned above. Therefore, the overall yield of the process is increased by producing fewer devices with defects and the particle contamination of wafer will be avoided also.

Fig 6 shows the system for the performing the process of the invention. First, the operator loads cassettes filled with wafers into the cassette indexer 75 which has two stages. Then the robot 85, located inside the loadlock chamber 88, moves the wafers one at a time from the cassette to slots in the storage elevator 80, which is also located inside the loadlock chamber 88. After the loadlock chamber 88 is pumped down to a low pressure, the robot 85 moves a wafer into chamber a 90 for depositing the nucleation layer, and then robot 85 transfers the nucleated wafer to chamber B95 for bulk deposition. When processing of the wafer is completed, the wafer transfer sequence is reversed and the wafer is moved out of the chamber B 95 to the cassette by through the storage elevator 80. Finish the operator can remove the cassette with wafers from the system.